UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,568	01/22/2002	Mou-Shiung Lin	JCLA8533	6093

7590 08/28/2002

J.C. Patents, Inc.
4 Venture, Suite 250
Irvine, CA 92618

EXAMINER
MITCHELL, JAMES M

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,568	LIN ET AL.	
	Examiner	Art Unit	
	James Mitchell	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election

1. Applicant's election without traverse of Group 1 Claims 1-60 and subsequent cancellation of Group 2 claims 61-138 in Paper No. 4 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5, 6-21, 25-30, 33-52 and 56-60 are rejected under 35 U.S.C. 102(b) as being anticipated by Akagawa (U.S 6,121,688).

4. Akagawa (Fig 6, 11) discloses a chip package structure comprising a silicon substrate (47), a plurality of die (32) with an active surface, a backside that is opposite to the active surface that inherently transmits, whereas the backside of the die is adhered to said substrate, and thin film circuit layer (38) located on top of the silicon substrate and die and has an external circuitry (46), wherein the external circuitry is electrically connected to the metal pads (36) of the die and extends to a region outside the active surface of the die, the external circuitry has a plurality of bonding pads (portion of wiring 40 in contact with external terminal) located on the thin film circuit layer and each bonding pad is electrically connected to a corresponding metal pad of the die; wherein a plurality of active devices located on the active surface of the die and the internal circuitry electrically connected; wherein the thin film circuit layer comprises a

patterned wiring layer (40), a dielectric layer (34) formed on top of the silicon substrate and the die and the wiring layer located on top of the dielectric layer, whereas the patterned wiring layer is electrically connected (via conductive material, 38) to the metal pad of the die through the inherent porous dielectric layer (opening in dielectric) and forms the external circuitry and the bonding pads of the external circuitry; wherein external circuitry further comprises an inherent power/ground bus (Column 8, Lines 32-36), a plurality of inherent through hole (via hole in dielectric) and the wiring is electrically connected to the metal pads of the die by the through hole comprising a via; the external circuitry further comprising a capacitor passive device formed by a part of the patterned wiring layer (Column 8, Lines 37-40); the thin film circuit layer comprising a plurality of patterned wiring layer and a plurality of dielectric layers (41; Fig 11) whereby the patterned wiring layer and dielectric layer are alternately formed and the patterned wiring layers are electrically connected to the neighboring pattern with vias (Column 9, Lines 20-21) with the wiring that is closest to the silicon substrate is electrically connected to the metal pads, and the wiring farthest away forms a bonding pad (portion in contact with bump, 46), the conductive material is an epoxy that fills a space between a surface of the silicon substrate and the thin film circuit layer, therefore it is a filler that is likewise planar to the active surface of the die, a passivation layer (41) on top of the thin film circuit layer and exposing bonding pads, a plurality of bonding point bump located on the bonding pads .

5. Claims 1,22,23, 30-32,53,54 rejected under 35 U.S.C. 102(b) as being anticipated by Shanefield (U.S 4,866,501).

6. Shanefield discloses a chip package structure comprising a silicon substrate (10), a plurality of die (11) with an active surface, a backside that is opposite to the active surface that inherently transmits, whereas the backside of the die is adhered to said substrate, and thin film circuit layer (17,24) located on top of the silicon substrate and die and has an external circuitry (19,25), wherein the external circuitry is electrically connected to the metal pads (20) of the die and extends to a region outside the active surface of the die, the external circuitry has a plurality of bonding pads (25) located on the thin film circuit layer and each bonding pad is electrically connected to a corresponding metal pad of the die; wherein the silicon substrate further comprises an inwardly protruded area (cavity portion) located on a surface of the silicon substrate where the backside of chip is adhered to a bottom of the inwardly protruded area, and a heat conducting layer (14) formed overlapping, a surface of the silicon substrate is a side of the heat conducting layer that is further away from the silicon layer, the silicon layer has at least one opening that penetrates through the silicon layer used to form the an inwardly protruded area and the backside is adhered to a bottom of the inwardly protruded area,; with the structure having dies that perform the same function and dies that perform different functions (Column 1, Lines 14-17).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 4 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akagawa as applied to claims 3 and 34.

10. Akagawa does not appear to disclose the width, length or thickness of the traces.

11. In any case, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc.,

725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

12. Claims 24 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shanefield as applied to claims 23 and 54.

13. Shanefield does not appear to explicitly show that the silicon substrate is approximately equal to a thickness of the dies. See paragraph 10.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Mitchell whose telephone number is (703) 305-0244. The examiner can normally be reached on M-F 10:30-8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3230 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmm
August 23, 2002

DAVID E. GRAYBILL
PRIMARY EXAMINER